AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior listing of claims in this application.

1. (Currently amended) A semiconductor inspection system, comprising:

a navigation system for storing design information such as [[CAD]] design data of a semiconductor chip and for setting capturing and inspecting conditions including a region on a semiconductor wafer subject to inspection based on the design information; and

a scanning electron microscope system for performing actual capturing of the semiconductor wafer and for executing inspection in accordance with the capturing and inspecting conditions being set,

wherein the navigation system sets a template comprising a bitmap based on the design information, and performs a matching process a pattern within a grayscale image provided by the scanning electron microscope, and wherein a portion of the image that corresponds to the template is re-registered as a new template in place of the bitmap based on the design information.

2. (Original) The semiconductor inspection system according to claim 1, wherein the navigation system includes a function to design semiconductor patterns by itself or a function to retrieve the design information from another navigation system connected via a network, said another navigation system possessing a designing function.

3. (Original) The semiconductor inspection system according to claim 1, wherein the navigation system specifies and retrieves desired design data out of the stored design information to display the design data on a display screen.

4. (Currently amended) The semiconductor inspection system according to claim 1, wherein the navigation system includes a function to specify and retrieve an arbitrary portion out of the [[CAD]] design data being the stored design information and to generate bitmap data therefrom.

5. (Currently amended) The semiconductor inspection system according to claim 1, wherein the navigation system has a function to effectuate automatic editing of all the capturing and inspecting conditions to be used in the scanning electron microscope system out of the design information including the [[CAD]] design data and to transmit the edited capturing and inspecting conditions to the scanning electron microscope system.

6. (Original) The semiconductor inspection system according to claim 1, wherein the navigation system has a function to effectuate transmission and receipt of data with another navigation system connected to a network of a facility installed and further to transmit the capturing and inspecting conditions to a plurality of the scanning electron microscope systems connected to the network.

7. (Original) The semiconductor inspection system according to claim 1,

wherein the navigation system comprises:

a bitmap data generator having a function to generate bitmap data by retrieving desired design data out of the stored design information; and

a capturing and inspecting condition editor having a function to edit and transmit the capturing and inspecting conditions to be used in the scanning electron microscope system out of the design data.

8. (Original) The semiconductor inspection system according to claim 1, wherein the navigation system has a function to automatically detect a characteristic pattern portion and to register the pattern portion as a template, in the case of selecting a template for matching out of bitmap data as one of the inspecting conditions to be used in the scanning electron microscope system.

9. (Original) The semiconductor inspection system according to claim 1,

wherein the scanning electron microscope system uses the capturing and inspecting conditions received from the navigation system,

the scanning electron microscope system obtains a scanning electron microscope image automatically, and

the scanning electron microscope system performs inspection.

10. (Original) The semiconductor inspection system according to claim 1,

wherein the scanning electron microscope system uses the capturing and inspecting conditions received from another navigation system connected via a network,

the scanning electron microscope system obtains a scanning electron microscope image automatically, and

the scanning electron microscope system performs inspection.

11. (Original) The semiconductor inspection system according to claim 1, wherein the scanning electron microscope system has a function for matching between

bitmap data generated from the design information and a scanning electron microscope image.

12. (Original) The semiconductor inspection system according to claim 11,

wherein the scanning electron microscope system comprises:

means for generating edge images by retrieving edge information severally from the scanning electron microscope image obtained by capturing and from a template being bitmap data in the case of performing a matching process with the scanning electron microscope image obtained by capturing using the bitmap data from the design data as a template; and

means for performing the matching process with respect to the edge images severally generated from the scanning electron microscope image and the template while providing the both images with a smoothing process severally so as to make up deformed parts of the both images.

13. (Original) The semiconductor inspection system according to claim 11, wherein the scanning electron microscope system retrieves edge information in accordance with multiple directions and generates edge images depending on the multiple directions in the case of generating edge images by retrieving edge information from a scanning electron microscope image and from a template being bitmap data,

the scanning electron microscope system generates the edge images depending on the multiple directions, and

the scanning electron microscope system performs a matching process with respect to each of the images.

14. (Original) The semiconductor inspection system according to claim 11, wherein the scanning electron microscope system performs a matching process by composing edge images generated in accordance with multiple directions and by integrating the edge images into one image in the case of generating edge images by retrieving edge information from a scanning electron microscope image and from a template being bitmap data.

15. (Original) The semiconductor inspection system according to claim 1,

wherein the scanning electron microscope system comprises:

means for generating an edge image by retrieving edge information from a scanning electron microscope image obtained by capturing in the case of performing a matching process between the scanning electron microscope image and bitmap data from the design information as a template;

means for re-registering a portion of the scanning electron microscope image as a template, said portion corresponding to a position of the edge image detected by the matching process between the edge image and design data; and

means for using the re-registered template of the scanning electron microscope image in the subsequent matching process.

16. (Original) The semiconductor inspection system according to claim 15, wherein the scanning electron microscope system carries out re-registration of the template during repeated capturing processes at an interval of an arbitrary period of time or an arbitrary frequency of the processes in the case that the scanning electron microscope system uses the re-registered template of the scanning electron microscope

image and performs the matching processes with respect to scanning electron microscope images repeatedly captured.

17. (Original) The semiconductor inspection system according to claim 15, wherein the scanning electron microscope system compares a correlation value between the design data and the scanning electron microscope image every time and re-registers a new template only when the compared correlation value is higher than the correlation value of the template used at that time.

18. (Original) The semiconductor inspection system according to claim 15,

wherein the scanning electron microscope system performs an arbitrary frequency of the matching processes initially,

the scanning electron microscope system compares correlation values between the design data and the scanning electron microscope images obtained in the arbitrary frequency of the matching processes, and

the scanning electron microscope system re-registers the scanning electron microscope image having the highest correlation value as a new template.

19. (Original) The semiconductor inspection system according to claim 1, wherein the capturing and inspecting conditions are selected from a capturing and inspecting condition file registered in advance with the navigation system or the scanning electron microscope system.

20. (Original) The semiconductor inspection system according to claim 19, wherein the capturing and inspecting conditions are selected from the capturing and inspecting condition file weighted in accordance with a frequency of use in the past.

21. (Original) The semiconductor inspection system according to claim 19, wherein a capturing and inspecting condition inside the capturing and inspecting condition file is automatically deleted from the capturing and inspecting condition file when a frequency of use of the capturing and deleting condition is lower than a predetermined frequency.

22. (Original) The semiconductor inspection system according to claim 19, further comprising:

a function to modify and to edit a part of the capturing and inspecting conditions inside the capturing and inspecting condition file, the capturing and inspecting condition file being registered in advance.

23. (Original) The semiconductor inspection system according to claim 19, further comprising:

a function to register a condition with the capturing and inspecting condition file as another condition when a part of the capturing and inspecting conditions inside the capturing and inspecting condition file being registered in advance is modified.

24. (Currently amended) A semiconductor inspection method by which a pattern within an image provided by a scanning electron microscope is determined by using a template that is registered in advance, the method comprising the steps of:

creating a template comprising a bitmap based on semiconductor chip design information such as [[CAD]] design data;

detecting, by a pattern matching process, a position in a grayscale image provided by the scanning electron microscope which corresponds to the template; and

re-registering an image portion corresponding to the detected position as a new template in place of the bitmap based on the design information.

25. (Currently amended) A semiconductor inspection comprising:

a navigation system for registering a template used for a matching process for the identification of a portion of a semiconductor wafer subject to inspection; and

a scanning electron microscope system for forming an image based on the irradiation of the semiconductor wafer with an electron beam;

wherein the navigation system sets the template comprising a bitmap based on semiconductor chip design information such as [[CAD]] design data, performs a matching process, by using the template, with respect to a pattern within an image provided by the scanning electron microscope system, and re-registers as a template a portion of the image that is detected by the matching process and which corresponds to the template whereby the template is matched with a pattern within a grayscale image, wherein a portion of the image provided by the scanning electron microscope that is detected by the matching process and which corresponds to the template is re-registered as a new template in place of the bitmap based on the design information for the pattern matching process.